Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-59 (Canceled)

Claim 60 (Currently amended): Electronic assembly, comprising:

a first plurality of semiconductor dies mounted edge-to-edge, in close proximity to one another, on a first side of a printed circuit board, each semiconductor die electrically connected to the printed circuit board by ~~free-standing, resilient~~ spring contact structures mounted to each of the semiconductor dies.

Claim 61 (Original): Electronic assembly, according to claim 60, wherein:

the semiconductor dies are memory devices.

Claim 62 (Original): Electronic assembly, according to claim 60, wherein:

the electronic assembly is a single in-line memory module (SIMM).

Claim 63 (Currently amended): Electronic assembly, according to claim 60, wherein:

the ~~resilient~~ contact structures are ~~compliant~~ elongate.

Claim 64 (Previously presented): Electronic assembly, according to claim 60 further comprising a second plurality of semiconductor dies mounted to a second side of the printed circuit board.

Claim 65 (Currently amended): Electronic assembly, according to claim 60, wherein the ~~freestanding resilient~~ contact structures comprise:

wires bonded to the semiconductor dies; and

an overcoat covering at least a portion of the wires.

Claim 66 (Currently amended): Electronic assembly, according to claim 60, wherein the ~~freestanding resilient~~ contact structures comprise plated wires adhered to the semiconductor dies.

Claim 67 (Canceled)

Claim 68 (Currently amended): Electronic assembly, according to claim 60, further comprising:

a rigidizing material encapsulating at least a portion of the ~~resilient~~ contact structures.

Claims 69-346 (Canceled)

Claim 347 (Currently amended): Semiconductor package, comprising:

a first insulating layer;

a first conductive layer disposed on a first surface of the first insulating layer and patterned to have a first plurality of conductive traces;

a second insulating layer disposed on said first conductive layer;

a second conductive layer disposed on a first surface of the second insulating layer and patterned to have a second plurality of conductive traces;

~~the first conductive layer being in contact with the second insulating layer;~~

the second conductive and insulating layers are arranged and disposed so that outer portions of the first plurality of conductive traces are exposed;

a first plurality of electrical contact structures mounted to outer portions of the first plurality of conductive traces; and

a second plurality of electrical contact structures mounted to the second plurality of conductive traces.

Claim 348 (Currently amended): Semiconductor package, according to claim 347, wherein:

the first plurality of electrical contact structures extend from the first plurality of conductive traces to a plane; and

the second plurality of electrical contact structures extend from the second plurality of conductive traces to the plane.

Claim 349 (Original): Semiconductor package, according to claim 347, wherein:

the first plurality of electrical contact structures are resilient contact structures; and

the second plurality of electrical contact structures are resilient contact structures.

Claim 350 (Currently amended): ~~Semiconductor package, according to claim 347, further comprising:~~ Semiconductor package, comprising:

a first insulating layer;

a first conductive layer disposed on a first surface of the first insulating layer and patterned to have a first plurality of conductive traces;

a second insulating layer;

a second conductive layer disposed on a first surface of the second insulating layer and patterned to have a second plurality of conductive traces;

the first conductive layer being in contact with the second insulating layer;

the second conductive and insulating layers are arranged and disposed so that outer portions of the first plurality of conductive traces are exposed;

a first plurality of electrical contact structures mounted to outer portions of the first plurality of conductive traces;

a second plurality of electrical contact structures mounted to the second plurality of conductive traces; and

means for receiving a semiconductor device;

wherein:

the second conductive and insulating layers are arranged and disposed so that inner portions of the first plurality of conductive traces are exposed for connecting to a semiconductor device; and

further comprising:

means for connecting the semiconductor device to the exposed inner portions of the first plurality of conductive traces; and

means for connecting the semiconductor device to the second plurality of conductive traces.

Claim 351 (Currently amended): Semiconductor device, comprising:

a semiconductor die having a front surface and a back surface;

a plurality of ~~free-standing~~ elongate, spring interconnect structures mounted to the front surface of the semiconductor die; and

a ~~plurality of free-standing~~ heat-dissipating ~~structures~~ structure mounted to the back surface of the semiconductor die.

Claim 352 (Currently amended): Semiconductor device, according to claim 351, ~~wherein: the interconnect structures are resilient contact structures~~ wherein the heat dissipating structure comprises:

a terminal, and

a wire repeatedly bonded to the terminal and forming a plurality of loops.

Claim 353 (Currently amended): Semiconductor device, according to ~~claim 351, wherein:~~

~~the interconnect structures are compliant contact structures~~ claim 352, wherein the wire forms a fence structure, and the heat dissipating structure further comprises solder disposed within the fence structure.

Claim 354 (Currently amended): Semiconductor device, according to claim 351, ~~wherein: the free-standing heat-dissipating structures are~~ wherein the heat dissipating structure comprises a plurality of wires ~~mounted~~ wirebonded to the back surface of the semiconductor die.

Claim 355 (Currently amended): Semiconductor device, according to ~~claim 351~~ claim 354, wherein:

the ~~free-standing~~ interconnect structures are of a first material; and

the ~~free-standing heat-dissipating structures~~ wires are of a second material which is different from the first material.

Claim 356 (Currently amended): Semiconductor device, according to ~~claim 355~~ claim 354, wherein:

the ~~free-standing~~ interconnect structures and the ~~free-standing heat-dissipating structures~~ wires are overcoated with a common material.

Claim 357 (Currently amended): Semiconductor device, according to ~~claim 351 further comprising:~~

~~a layer of a metallic material disposed between the free-standing heat-dissipating structures and the back surface of the semiconductor die~~ claim 354, wherein the back surface of the semiconductor die comprises a conductive layer to which the wires are bonded.

Claim 358 (Currently amended): Semiconductor device, comprising:

a semiconductor die having a front surface and a back surface; and

a plurality of ~~free-standing resilient~~ spring contact structures mounted to the front surface of the semiconductor die.

Claim 359 (Original): Semiconductor device, according to claim 358, further comprising:

conductive pads disposed on the front surface of the semiconductor die; and wherein:

one contact structure is mounted to each conductive pad.

Claim 360 (Currently amended): Semiconductor device, according to claim 358, wherein the ~~resilient~~ contact structures each comprise:

a wire stem bonded at one end to the front surface of the semiconductor die and configured to have a springable shape; and

an overcoat material applied over the wire stem and over a portion of the front surface of the semiconductor die.

Claim 361 (Currently amended): Semiconductor device, according to claim 358, wherein:

the ~~resilient~~ contact structures are ~~compliant~~ elongate.

Claims 362-374 (Canceled)

REMARKS/ARGUMENTS

Claims 60, 63, 65, 66, 68, 347, 348, 350-358, 360, and 361 have been amended. Claims 60-66, 68, and 347-361 remain pending in the application. (Claims 1-59, 67, 69-346, and 362-374 were previously cancelled.) Applicants respectfully request reexamination and reconsideration of the application.

Applicants acknowledge with appreciation the Examiner's indication that claim 350 contains allowable subject matter. Claim 350 has been rewritten in independent form, as suggested by the Examiner, and should now be in condition for allowance.

Claims 60-64 were rejected as anticipated by U.S. Patent No. 5,255,431 to Burdick ("Burdick"), and claims 65, 66, and 68 were rejected as obvious in view of Burdick in combination with US Patent No. 4,667,219 to Lee et al. ("Lee"). Applicants respectfully traverse these rejections.

Independent claim 60 describes a plurality of semiconductor dice in which each die is connected to a printed circuit board by "spring contact structures," which are mounted to the semiconductor dice. Burdick's pins 66 are not springs, and nothing in Burdick suggests replacing the rigid pins 66 with springs. In addition, element 60 is not a plurality of semiconductor dice but is the planar surface of an HDI overcoat 44. (See Burdick col. 7, lines 57-68.) Nor are elements 22 semiconductor dice; rather, elements 22 are DIP components. (See Burdick col. 7, lines 13-25.) For both of these reasons, independent claim 60 patentably distinguishes over Burdick. Claims 61-64 depend from claim 60 and therefore also patentably distinguish over Burdick.

Claims 65 and 66 describe the spring contact structures as, respectively, comprising an overcoated or plated wire, and claim 68 includes "a rigidizing material encapsulating at least a portion of the contact structures." Because Burdick does not show any type of coating, plating, or encapsulant on pins 66, Lee is cited. Nowhere, however, does Lee teach or suggest any coating, plating, or encapsulant on wires 84. The rectangular box outlining each of wires 84 in Figure 9 is not described anywhere in Lee as a coating, plating, or encapsulant. It is most likely solder 88, which attaches the ends of wires 84 to terminals of power plane 24, as shown in Figure 8. (See Lee col., 4, line 58 to col. 5, line 5.) Therefore, even if combined, Burdick and Lee fail to meet the coating, plating, or encapsulate features of claims 65, 66, and 68. For this additional reason, those claims patentably distinguish over Burdick and Lee.

Claims 347-349 were rejected as anticipated by US Patent No. 5,317,479 to Pai et al. ("Pai"). Applicants respectfully traverse this rejection.

Independent claim 347 states that the second insulating layer is disposed on the first conductive layer. Multichip module 90, which the Examiner equates with the second insulating layer 90, is not disposed on the board contacts 57, which the Examiner equates with the first conductive layer. Nor is there any motivation or suggestion to modify Pai such that the multichip module 90 is disposed on the board contacts 57. Indeed, to make such a modification would destroy the purpose of the Pai invention, leaving no room between multichip module 90 and circuit board 54 for IC chips 92, 94. Therefore, independent claim 347 patentably distinguishes over Pai.

Claims 348 and 349 depend from claim 347 and therefore also patentably distinguish over Pai. In addition, claim 349 describes both the first contact structures and the second contact structures as extending from the respective conductive traces to which they are attached to the same plane. In contrast, the plane to which leads 50 in Pai (which the Examiner equates with the first contact structures) extend is the chip contact 57 (which the Examiner equates with the second conductive traces). As shown in Figure 5B, the leads to chips 92, 94 (which the Examiner equates with the second contact structures) do not extend from the chip contact 57 to the same plane, which would have to be back to the chip contact 57. Therefore, dependent claim 349 further distinguishes over Pai.

Claims 351-357 were rejected as obvious in view of the combination of Lee and US Patent No. 5,265,321 to Nelson et al. ("Nelson"). Applicants respectfully traverse this rejection.

Independent claim 351 includes a plurality of "elongate, ***spring*** interconnect structures." Copper wires, such as those disclosed as element 84 in Figure 8 of Lee, are not ***spring*** interconnect structures. Nothing in Lee describes wires 84 as springs, and indeed, a bare copper wire is not a spring. Nelson similarly fails to disclose any sort of elongate, spring interconnect structure. Nor does any teaching in Lee or Nelson suggest or provide any motivation for replacing wires 84 in Lee with springs. Therefore, independent claim 351 patentably distinguishes over Lee and Nelson.

Claims 352-357 depend from claim 351 and therefore also patentably distinguish over Lee and Nelson. Moreover, claims 352-357 describe additional features that further distinguish over Lee and Nelson. For example, claim 352 describes the heat-dissipating structure as

comprising a terminal to which a wire is repeatedly bonded forming loops. Claim 353 further describes the wire as forming a fence structure into which solder is disposed. Neither Lee nor Nelson teach or suggest such features.

As another example, claim 354 describes the heat-dissipating structure as comprising a plurality of wires wirebonded to the back surface of the semiconductor die. Because wires and wirebonding equipment are commonly used in packaging semiconductor dice, it is convenient and saves time to form the heat-dissipating structure out of wires bonded to the back surface of the die. The pins 20 shown in Nelson are not wires and are not wirebonded. Nelson's pins 20, therefore, are not as advantageous as wires that are wirebonded. The wirebonded wires of claim 354 thus represent an improvement over the pins 20 of Nelson. Claim 354 therefore patentably distinguishes over Lee and Nelson.

Applicants respectfully traverse the statement that overcoating both the interconnection structures and the wires that compose the heat-dissipating structure with a common material would have been obvious because overcoating would further increase the thermal conduction properties of the wires. There is no evidence that overcoating would increase the thermal conductive properties of the wires. For example, how does overcoating the interconnection structures increase the thermal conductive properties of the wires? Moreover, the motivation to modify a reference must come from the prior art. Here, however, there is no teaching or suggestion in either Lee or Nelson that ovecoating both interconnection structures and the heat-dissipating structure with the same material would improve thermal conduction. Therefore, claim 356 further distinguishes over Lee and Nelson.

Claims 358-361 were rejected as anticipated by Lee. Applicants respectfully traverse this rejection.

Independent claim 358 describes the contact structures mounted to the semiconductor die as springs. As discussed above, bare copper wires, such as those disclosed as element 84 in Figure 8 of Lee, are not springs, nor does any teaching in Lee suggest or provide any motivation for replacing copper wires 84 in Lee with springs. Therefore, independent claim 358 patentably distinguishes over Lee.

Claims 359-361 depend from claim 358 and therefore also patentably distinguishes over Lee. In addition, Applicants traverse the conclusion that Lee discloses overcoating wires 84. As discussed above, the rectangular box outlining each of wires 84 in Figure 9 is not described

anywhere in Lee as an overcoat. Rather, it is most likely solder 88, which attaches the ends of wires 84 to terminals power plane 24, as shown in Figure 8. (See Lee col., 4, line 58 to col. 5, line 5.)

In view of the foregoing, Applicants submit that all of the claims are allowable and the application is in condition for allowance. If the Examiner believes that a discussion with Applicants' attorney would be helpful, the Examiner is invited to contact the undersigned at (801) 536-6763.

Respectfully submitted,

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